WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a complementary PWM signal generation unit for generating a first PWM signal and a second PWM signal corresponding to an inverted signal of said first PWM signal; and

a dead time addition unit for adding a first dead time at a rise of said first PWM signal and a second dead time at a rise of said second PWM signal,

wherein said first dead time and said second dead time are individually settable in said dead time addition unit.

2. The semiconductor device of Claim 1,

wherein said dead time addition unit includes:

a dead time timer; and

first and second dead time set registers, and

time elapsing until a value of said dead time timer reaches a set value of said first dead time set register is set as said first dead time, and time elapsing until the value of said dead time timer reaches a set value of said second dead time set register is set as said second dead time.

3. The semiconductor device of Claim 2,

wherein said first and second dead time set registers are serially disposed.

4. The semiconductor device of Claim 2,

wherein said first and second dead time set registers are disposed in parallel.

5. The semiconductor device of Claim 1,

wherein said dead time addition unit includes:

first and second dead time timers; and

first and second dead time set registers, and

time elapsing until a value of said first dead time timer reaches a set value of said first dead time set register is set as said first dead time, and time elapsing until a value of said second dead time timer reaches a set value of said second dead time set register is set as said second dead time.

6. The semiconductor device of Claim 1,

wherein said dead time addition unit includes:

first and second dead time set registers; and

a comparator for comparing a count value of a cycle counter included in said complementary PWM generation unit with set values of said first and second dead time set registers, and

said first dead time is set on the basis of a result of comparison by said comparator with the set value of said first dead time set register, and said second dead time is set on the basis of a result of comparison by said comparator with the set value of said second dead time set register.

7. The semiconductor device of Claim 1,

wherein said dead time addition unit includes:

first and second dead time set registers;

a first comparator for comparing a count value of a cycle timer with a set value of said first dead time set register; and

a second comparator for comparing the count value of said cycle timer with a set value of said second dead time set register, and

said first dead time is set on the basis of a result of comparison by said first comparator and said second dead time is set on the basis of a result of comparison by said second comparator.

8. The semiconductor device of Claim 1,

wherein at least one of said first and second dead times is changeable in accordance with a dead time switching input.

9. A control method employed in an induction heating apparatus,

said induction heating apparatus including an inverter circuit for performing a heating operation with a coil and the semiconductor device of Claim 8 for controlling said inverter circuit by supplying said first and second PWM signals to which dead times have been added,

the control method comprising the steps of:

said inverter circuit supplying a signal to said semiconductor device as said dead time switching input; and

said semiconductor device changing at least one of said first and second dead times in accordance with said supplied dead time switching input.

10. The control method of Claim 9,

wherein said inverter circuit outputs an abnormal signal corresponding to abnormal heating as said dead time switching input, and

said semiconductor device changes at least one of said first and second dead times when said abnormal signal is accepted.

11. The control method of Claim 9,

wherein said inverter circuit outputs an analog signal corresponding to a current value of a heating coil current as said dead time switching input, and

said semiconductor device subjects said supplied analog signal to AD conversion and changes at least one of said first and second dead times when a value resulting from the AD conversion is out of a given range.